CLAIMS

1. A semiconductor device comprising:

an insulating underlayer;

a first insulating interlayer formed on said insulating underlayer, said first insulating interlayer having a groove;

a first silicon-diffused metal layer buried in said groove; and

a first metal diffusion barrier layer formed on said first silicon-diffused metal layer and said first insulating interlayer.

2. The device as set forth in claim 1, wherein said first insulating interlayer comprises at least one of a SiO_2 layer, a SiCN layer, a SiC layer, a SiOC layer and a low-k material layer.

3. The device as set forth in claim 2, wherein said low-k material layer comprises one of a ladder-type hydrogen siloxane layer and a porous ladder-type hydrogen siloxane layer.

4. The device as set forth in claim 3, wherein said ladder-type hydrogen siloxane layer comprises an L-Ox™ layer.

5. The device as set forth in claim 3, wherein said ladder-type hydrogen siloxane layer has a density of about 1.50 g/cm^3 to 1.58 g/cm^3.

6. The device as set forth in claim 3, wherein said ladder-type hydrogen siloxane layer has a refractive index of about 1.38 to 1.40 at a wavelength of about 633 nm.

7. The device as set forth in claim 3, further comprising a mask insulating layer made of silicon dioxide formed on the one of said ladder-type hydrogen siloxane layer and said porous ladder-type hydrogen siloxane layer.

8. The device as set forth in claim 1, wherein said

first silicon-diffused metal layer has a larger silicon concentration near an upper side thereof than near a lower side thereof.

9. The device as set forth in claim 1, wherein said first silicon-diffused metal layer comprises a silicon-diffused copper layer.

10. The device as set forth in claim 9, wherein a silicon component of said silicon-diffused copper layer is less than 8 atoms %.

11. The device as set forth in claim 1, wherein said first silicon-diffused metal layer comprises a silicon-diffused copper alloy layer including at least one of Al, Ag, W, Mg, Fe, Ni, Zn, Pd, Cd, Au, Hg, Be, Pt, Zr, Ti and Sn.

12. The device as set forth in claim 1, wherein said first silicon-diffused metal layer includes no metal silicide.

13. The device as set forth in claim 1, wherein said first silicon-diffused metal layer includes hydrogen.

14. The device as set forth in claim 1, wherein said first silicon-diffused metal layer includes carbon.

15. The device as set forth in claim 1, wherein said first metal diffusion barrier layer comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

16. The device as set forth in claim 1, further comprising a first etching stopper between said insulating underlayer and said first insulating interlayer.

17. The device as set forth in claim 16, wherein said first etching stopper comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

18. The device as set forth in claim 1, further comprising:

a second insulating interlayer formed on said first metal diffusion barrier layer, said second insulating interlayer and said first metal diffusion barrier layer having a via hole opposing said groove of said first insulating interlayer;

a second silicon-diffused metal layer buried in said via hole;

a second metal diffusion barrier layer formed on said second silicon-diffused metal layer and said second insulating interlayer;

a third insulating interlayer formed on said second metal diffusion barrier layer, said third insulating interlayer and said second metal diffusion barrier layer having a trench opposing said via hole;

a third silicon-diffused metal layer buried in said trench; and

a third metal diffusion barrier layer formed on said third silicon-diffused metal layer and said third insulating interlayer.

19. The device as set forth in claim 18, wherein each of said second and third insulating interlayers comprises at least one of a SiO_2 layer, a SiCN layer, a SiC layer, a SiOC layer and a low-k material layer.

20. The device as set forth in claim 19, wherein said low-k material layer comprises one of a ladder-type hydrogen siloxane layer and a porous ladder-type hydrogen siloxane layer.

21. The device as set forth in claim 20, wherein said ladder-type hydrogen siloxane layer comprises an L-Ox™ layer.

22. The device as set forth in claim 20, wherein said ladder-type hydrogen siloxane layer has a density of about 1.50 g/cm^3 to 1.58 g/cm^3.

23. The device as set forth in claim 20, wherein said

ladder-type hydrogen siloxane layer has a refractive index of about 1.38 to 1.40 at a wavelength of about 633 nm.

24. The device as set forth in claim 20, further comprising a mask insulating layer made of silicon dioxide formed on the one of said ladder-type hydrogen siloxane layer and said porous ladder-type hydrogen siloxane layer.

25. The device as set forth in claim 18, wherein each of said second and third silicon-diffused metal layers has a larger silicon concentration near an upper side thereof than near a lower side thereof.

26. The device as set forth in claim 18, wherein each of said second and third silicon-diffused metal layers comprises a silicon-diffused copper layer.

27. The device as set forth in claim 26, wherein a silicon component of said silicon-diffused copper layer is less than 8 atoms %.

28. The device as set forth in claim 18, wherein each of said second and third silicon-diffused metal layers comprises a silicon-diffused copper alloy layer including at least one of Al, Ag, W, Mg, Fe, Ni, Zn, Pd, Cd, Au, Hg, Be, Pt, Zr, Ti and Sn.

29. The device as set forth in claim 18, wherein each of said second and third metal diffusion barrier layers comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

30. The device as set forth in claim 18, wherein each of said second and third silicon-diffused metal layers includes no metal silicide.

31. The device as set forth in claim 18, wherein each of said second and third silicon-diffused metal layers includes hydrogen.

32. The device as set forth in claim 18, wherein each of said second and third silicon-diffused metal layers

includes carbon.

33. The device as set forth in claim 1, further comprising:

a second insulating interlayer formed on said first metal diffusion barrier layer, said second insulating interlayer and said first metal diffusion barrier layer having a via hole opposing said groove of said first insulating interlayer;

a third insulating interlayer formed on said second insulating interlayer, said third insulating interlayer having a trench opposing said via hole;

a second silicon-diffused metal layer buried in said trench and said via hole; and

a second metal diffusion barrier layer formed on said second silicon-diffused metal layer and said third insulating interlayer.

34. The device as set forth in claim 33, wherein said second insulating interlayer comprises at least one of a SiO_2 layer, a SiCN layer, a SiC layer, a SiOC layer and a low-k material layer.

35. The device as set forth in claim 34, wherein said low-k material layer comprises one of a ladder-type hydrogen siloxane layer and a porous ladder-type hydrogen siloxane layer.

36. The device as set forth in claim 35, wherein said ladder-type hydrogen siloxane layer comprises an L-Ox™ layer.

37. The device as set forth in claim 35, wherein said ladder-type hydrogen siloxane layer has a density of about 1.50 g/cm^3 to 1.58 g/cm^3.

38. The device as set forth in claim 35, wherein said ladder-type hydrogen siloxane layer has a refractive index of about 1.38 to 1.40 at a wavelength of about 633 nm.

39. The device as set forth in claim 35, further

comprising a mask insulating layer made of silicon dioxide formed on the one of said ladder-type hydrogen siloxane layer and said porous ladder-type hydrogen siloxane layer.

40. The device as set forth in claim 33, wherein said second silicon-diffused metal layer has a larger silicon concentration near an upper side thereof than near a lower side thereof.

41. The device as set forth in claim 33, wherein said second silicon-diffused metal layer comprises a silicon-diffused copper layer.

42. The device as set forth in claim 41, wherein a silicon component of said silicon-diffused copper layer is less than 8 atoms %.

43. The device as set forth in claim 33, wherein said second silicon-diffused metal layer comprises a silicon-diffused copper alloy layer including at least one of Al, Ag, W, Mg, Fe, Ni, Zn, Pd, Cd, Au, Hg, Be, Pt, Zr, Ti and Sn.

44. The device as set forth in claim 33, wherein said second silicon-diffused metal layer includes no metal silicide.

45. The device as set forth in claim 33, wherein said second silicon-diffused metal layer includes hydrogen.

46. The device as set forth in claim 33, wherein said second silicon-diffused metal layer includes carbon.

47. The device as set forth in claim 33, wherein said second metal diffusion barrier layer comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

48. The device as set forth in claim 33, further comprising a second etching stopper between said second and third insulating interlayers, said second etching stopper having a trench opposing said trench.

49. The device as set forth in claim 48, wherein said second etching stopper comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

50. A semiconductor device comprising:

an insulating underlayer;

a first insulating interlayer formed on said insulating underlayer, said first insulating interlayer having a groove;

a first silicon-diffused metal layer including no metal silicide and buried in said groove;

a first metal diffusion barrier layer formed on said first silicon-diffused metal layer and said first insulating interlayer.

a second insulating interlayer formed on said first metal diffusion barrier layer, said second insulating interlayer and said first metal diffusion barrier layer having a via hole opposing said groove of said first insulating interlayer;

a metal layer buried in said via hole;

a second metal diffusion barrier layer formed on said metal layer and said second insulating interlayer;

a third insulating interlayer formed on said second metal diffusion barrier layer, said third insulating interlayer and said second metal diffusion barrier layer having a trench opposing said via hole;

a second silicon-diffused metal layer including no metal silicide and buried in said trench; and

a third metal diffusion barrier layer formed on said second silicon-diffused metal layer and said third insulating interlayer.

51. A semiconductor device comprising:

an insulating underlayer;

an insulating interlayer formed on said insulating underlayer, said insulating interlayer having a groove;

a barrier metal layer made of at least one of Ta, TaN, Ti, TiN, TaSiN and TiSiN formed within said groove;

a silicon-diffused copper layer including no copper silicide and buried in said groove on said barrier metal layer, said silicon-diffused copper layer having a silicon component of less than 8 atoms %; and

a copper diffusion barrier layer made of at least one of SiCN, SiC, SiOC and organic material and formed on said silicon-diffused copper layer and said insulating interlayer.

52. A semiconductor device comprising:

an insulating underlayer;

a first insulating interlayer formed on said insulating underlayer, said first insulating interlayer having a groove;

a first barrier metal layer made of at least one of Ta, TaN, Ti, TiN, TaSiN and TiSiN formed within said groove;

a first silicon-diffused copper layer including no copper silicide and buried in said groove on said first barrier metal layer, said first silicon-diffused copper layer having a silicon component of less than 8 atoms %;

a first copper diffusion barrier layer made of at least one of SiCN, SiC, SiOC and organic material and formed on said first silicon-diffused copper layer and said first insulating interlayer;

a second insulating interlayer formed on said first copper diffusion barrier layer, said second insulating interlayer having a via hole opposing said groove;

a second barrier metal layer made of at least

one of Ta, TaN, Ti, TiN, TaSiN and TiSiN formed within said via hole;

a second silicon-diffused copper layer including no copper silicide and buried in said via hole on said second barrier metal layer, said second silicon-diffused copper layer having a silicon component of less than 8 atoms %;

a second copper diffusion barrier layer made of at least one of SiCN, SiC, SiOC and organic material and formed on said second silicon-diffused copper layer and said second insulating interlayer;

a third insulating interlayer formed on said second insulating underlayer, said third insulating interlayer having a trench opposing said via hole;

a third barrier metal layer made of at least one of Ta, TaN, Ti, TiN, TaSiN and TiSiN formed within said trench;

a third silicon-diffused copper layer including no copper silicide and buried in said trench on said third barrier metal layer, said third silicon-diffused copper layer having a silicon component of less than 8 atoms %; and

a third copper diffusion barrier layer made of at least one of SiCN, SiC, SiOC and organic material and formed on said third silicon-diffused copper layer and said third insulating interlayer.

53. A semiconductor device comprising:

an insulating underlayer;

a first insulating interlayer formed on said insulating underlayer, said first insulating interlayer having a groove;

a first barrier metal layer made of at least one of Ta, TaN, Ti, TiN, TaSiN and TiSiN formed within said groove;

a first silicon-diffused copper layer

including no copper silicide and buried in said groove on said first barrier metal layer, said first silicon-diffused copper layer having a silicon component of less than 8 atoms %;

a first copper diffusion barrier layer made of at least one of SiCN, SiC, SiOC and organic material and formed on said first silicon-diffused copper layer and said first insulating interlayer;

a second insulating interlayer formed on said first copper diffusion barrier layer, said second insulating interlayer having a via hole opposing said groove;

a third insulating interlayer formed on said second insulating underlayer, said third insulating interlayer having a trench opposing said via hole;

a second barrier metal layer made of at least one of Ta, TaN, Ti, TiN, TaSiN and TiSiN formed within said trench and said via hole;

a second silicon-diffused copper layer including no copper silicide and buried in said trench and said via hole on said second barrier metal layer, said second silicon-diffused copper layer having a silicon component of less than 8 atoms %; and

a second copper diffusion barrier layer made of at least one of SiCN, SiC, SiOC and organic material and formed on said second silicon-diffused copper layer and said third insulating interlayer.

54. A method for manufacturing a semiconductor device, comprising the steps of:

forming a first groove in a first insulating interlayer;

burying a first metal layer in said groove;

diffusing first silicon into said first metal layer from an upper surface thereof so that said first metal layer is converted into a first silicon-diffused metal layer;

and

forming a first metal diffusion barrier layer on said first silicon-diffused metal layer and said first insulating interlayer.

55. The method as set forth in claim 54, wherein said first insulating interlayer comprises at least one of a SiO_2 layer, a SiCN layer, a SiC layer, a SiOC layer and a low-k material layer.

56. The method as set forth in claim 55, wherein said low-k material layer comprises one of a ladder-type hydrogen siloxane layer and a porous ladder-type hydrogen siloxane layer.

57. The method as set forth in claim 56, wherein said ladder-type hydrogen siloxane layer comprises an L-Ox™ layer.

58. The method as set forth in claim 56, wherein said ladder-type hydrogen siloxane layer has a density of about 1.50 g/cm^3 to 1.58 g/cm^3.

59. The method as set forth in claim 56, wherein said ladder-type hydrogen siloxane layer has a refractive index of about 1.38 to 1.40 at a wavelength of about 633 nm.

60. The method as set forth in claim 56, further comprising a step of forming a mask insulating layer made of silicon dioxide on the one of said ladder-type hydrogen siloxane layer and said porous ladder-type hydrogen siloxane layer.

61. The method as set forth in claim 54, wherein said first silicon-diffused metal layer has a larger silicon concentration near an upper side thereof than near a lower side thereof.

62. The method as set forth in claim 54, wherein said first silicon-diffused metal layer comprises a silicon-diffused copper layer.

63. The method as set forth in claim 62, wherein a

silicon component of said silicon-diffused copper layer is less than 8 atoms %.

64. The method as set forth in claim 54, wherein said first silicon-diffused metal layer comprises a silicon-diffused copper alloy layer including at least one of Al, Ag, W, Mg, Fe, Ni, Zn, Pd, Cd, Au, Hg, Be, Pt, Zr, Ti and Sn.

65. The method as set forth in claim 54, wherein said first metal diffusion barrier layer comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

66. The method as set forth in claim 54, further comprising a step of forming a first etching stopper between said insulating underlayer and said first insulating interlayer.

67. The method as set forth in claim 66, wherein said first etching stopper comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

68. The method as set forth in claim 54, wherein said first silicon diffusing step comprises the steps of:

reducing first oxide on said first metal layer; and

exposing said first metal layer with silicon-including gas so that said first metal layer is converted into said first silicon-diffused metal layer.

69. The method as set forth in claim 54, wherein said first silicon diffusing step comprises the steps of:

coating a first oxidation preventing layer on said first metal layer;

removing said first oxidation preventing layer; and

exposing said first metal layer with silicon-including gas so that said first metal layer is

converted into said first silicon-diffused metal layer after or when said first oxidation preventing layer is removed.

70. The method as set forth in claim 69, wherein said silicon-including gas includes inorganic silane gas.

71. The method as set forth in claim 70, wherein said inorganic silane gas includes at least one of SiH_4 gas, Si_2H_6 gas and SiH_2Cl_2 gas.

72. The method as set forth in claim 69, wherein said first oxidation preventing layer comprises a benzotriazole layer.

73. The method as set forth in claim 69, further comprising a step of reducing first oxide on said first metal layer, before said first oxidation preventing layer is coated.

74. The method as set forth in claim 73, wherein said first oxide reducing step uses oxalic acid.

75. The method as set forth in claim 69, wherein said first oxidation preventing layer removing step, said first silicon-including gas exposing step and said first metal diffusion barrier layer forming step are carried out in the same processing apparatus without exposing said semiconductor device to the air.

76. The method as set forth in claim 72, wherein said first oxidation preventing layer removing step is carried out at a temperature of about 250 to 400℃.

77. The method as set forth in claim 72, wherein said first silicon-including gas exposing step is carried out at a temperature of about 250 to 400℃.

78. The method as set forth in claim 72, wherein said first oxidation preventing layer removing step and said first silicon-including gas exposing step are simultaneously carried out at a temperature of about 250 to 400℃ in the same processing apparatus using said silicon-including gas.

79. The method as set forth in claim 54, wherein said

first silicon-diffused metal layer includes no metal silicide.

80. The method as set forth in claim 54, wherein said first silicon-diffused metal layer includes hydrogen.

81. The method as set forth in claim 54, wherein said first silicon-diffused metal layer includes carbon.

82. The method as set forth in claim 54, further comprising the steps of:

forming a second insulating interlayer on said first metal diffusion barrier layer, said second insulating interlayer and said first metal diffusion barrier layer having a via hole opposing said groove of said first insulating interlayer;

burying a second metal layer in said via hole;

diffusing second silicon into said second metal layer from an upper surface thereof so that said second metal layer is converted into a second silicon-diffused metal layer;

forming a second metal diffusion barrier layer on said second silicon-diffused metal layer and said second insulating interlayer;

forming a third insulating interlayer on said second metal diffusion barrier layer, said third insulating interlayer and said second metal diffusion barrier layer having a trench opposing said via hole;

burying a third metal layer in said trench;

diffusing third silicon into said third metal layer from an upper surface thereof so that said third metal layer is converted into a third silicon-diffused metal layer; and

forming a third metal diffusion barrier layer on said third silicon-diffused metal layer and said third insulating interlayer.

83. The method as set forth in claim 82, wherein each of said second and third insulating interlayers comprises at least one of a SiO_2 layer, a SiCN layer, a SiC layer, a SiOC layer and a low-k material layer.

84. The method as set forth in claim 83, wherein said low-k material layer comprises one of a ladder-type hydrogen siloxane layer and a porous ladder-type hydrogen siloxane layer.

85. The method as set forth in claim 84, wherein said ladder-type hydrogen siloxane layer comprises an L-Ox™ layer.

86. The method as set forth in claim 84, wherein said ladder-type hydrogen siloxane layer has a density of about 1.50 g/cm^3 to 1.58 g/cm^3.

87. The method as set forth in claim 84, wherein said ladder-type hydrogen siloxane layer has a refractive index of about 1.38 to 1.40 at a wavelength of about 633 nm.

88. The method as set forth in claim 84, further comprising a forming a mask insulating layer made of silicon dioxide on the one of said ladder-type hydrogen siloxane layer and said porous ladder-type hydrogen siloxane layer.

89. The method as set forth in claim 82, wherein each of said second and third silicon-diffused metal layers has a larger silicon concentration near an upper side thereof than near a lower side thereof.

90. The method as set forth in claim 82, wherein each of said second and third silicon-diffused metal layers comprises a silicon-diffused copper layer.

91. The method as set forth in claim 90, wherein a silicon component of said silicon-diffused copper layer is less than 8 atoms %.

92. The method as set forth in claim 82, wherein each of said second and third silicon-diffused metal layer comprises a silicon-diffused copper alloy layer including at

least one of Al, Ag, W, Mg, Fe, Ni, Zn, Pd, Cd, Au, Hg, Be, Pt, Zr, Ti and Sn.

93. The method as set forth in claim 82, wherein each of said second and third metal diffusion barrier layers comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

94. The method as set forth in claim 82, wherein said second silicon diffusing step comprises the steps of:

reducing second oxide on said second metal layer; and

exposing said second metal layer with silicon-including gas so that said second metal layer is converted into said second silicon-diffused metal layer.

95. The method as set forth in claim 82, wherein said second silicon diffusing step comprises the steps of:

coating a second oxidation preventing layer on said second metal layer;

removing said second oxidation preventing layer; and

exposing said second metal layer with silicon-including gas so that said second metal layer is converted into said second silicon-diffused metal layer after or when said second oxidation preventing layer is removed.

96. The method as set forth in claim 95, wherein said silicon-including gas includes inorganic silane gas.

97. The method as set forth in claim 96, wherein said inorganic silane gas includes at least one of SiH_4 gas, Si_2H_6 gas and SiH_2Cl_2 gas.

98. The method as set forth in claim 95, wherein said second oxidation preventing layer comprises a benzotriazole layer.

99. The method as set forth in claim 95, further comprising a step of reducing second oxide on said second metal

layer, before said second oxidation preventing layer is coated.

100. The method as set forth in claim 99, wherein said second oxide reducing step uses oxalic acid.

101. The method as set forth in claim 95, wherein said second oxidation preventing layer removing step, said second silicon-including gas exposing step and said second metal diffusion barrier layer forming step are carried out in the same processing apparatus without exposing said semiconductor device to the air.

102. The method as set forth in claim 98, wherein said second oxidation preventing layer removing step is carried out at a temperature of about 250 to 400°C.

103. The method as set forth in claim 98, wherein said second silicon-including gas exposing step is carried out at a temperature of about 250 to 400°C.

104. The method as set forth in claim 98, wherein said second oxidation preventing layer removing step and said second silicon-including gas exposing step are simultaneously carried out at a temperature of about 250 to 400°C in the same processing apparatus using said silicon-including gas.

105. The method as set forth in claim 82, wherein said second silicon-diffused metal layer includes no metal silicide.

106. The method as set forth in claim 82, wherein said second silicon-diffused metal layer includes hydrogen.

107. The method as set forth in claim 82, wherein said second silicon-diffused metal layer includes carbon.

108. The method as set forth in claim 82, wherein said third silicon diffusing step comprises the steps of:

reducing third oxide on said third metal layer; and

exposing said third metal layer with

silicon-including gas so that said third metal layer is converted into said third silicon-diffused metal layer.

109. The method as set forth in claim 82, wherein said third silicon diffusing step comprises the steps of:

coating a third oxidation preventing layer on said third metal layer;

removing said third oxidation preventing layer; and

exposing said third metal layer with silicon-including gas so that said third metal layer is converted into said third silicon-diffused metal layer after or when said third oxidation preventing layer is removed.

110. The method as set forth in claim 109, wherein said silicon-including gas includes inorganic silane gas.

111. The method as set forth in claim 110, wherein said inorganic silane gas includes at least one of SiH_4 gas, Si_2H_6 gas and SiH_2Cl_2 gas.

112. The method as set forth in claim 109, wherein said third oxidation preventing layer comprises a benzotriazole layer.

113. The method as set forth in claim 109, further comprising a step of reducing third oxide on said third metal layer, before said third oxidation preventing layer is coated.

114. The method as set forth in claim 113, wherein said third oxide reducing step uses oxalic acid.

115. The method as set forth in claim 109, wherein said third oxidation preventing layer removing step, said third silicon-including gas exposing step and said third metal diffusion barrier layer forming step are carried out in the same processing apparatus without exposing said semiconductor device to the air.

116. The method as set forth in claim 112, wherein said third oxidation preventing layer removing step is carried out

at a temperature of about 250 to 400°C.

117. The method as set forth in claim 112, wherein said third silicon-including gas exposing step is carried out at a temperature of about 250 to 400°C.

118. The method as set forth in claim 112, wherein said third oxidation preventing layer removing step and said third silicon-including gas exposing step are simultaneously carried out at a temperature of about 250 to 400°C in the same processing apparatus using said silicon-including gas.

119. The method as set forth in claim 82, wherein said third silicon-diffused metal layer includes no metal silicide.

120. The method as set forth in claim 82, wherein said third silicon-diffused metal layer includes hydrogen.

121. The method as set forth in claim 82, wherein said third silicon-diffused metal layer includes carbon.

122. The method as set forth in claim 54, further comprising the steps of:

forming second and third insulating interlayers on said first metal diffusion barrier layer;

forming a via hole in said third and second insulating interlayers, said via hole opposing said groove of said first insulating interlayer;

forming a trench in said third insulating interlayer, said trench opposing said via hole;

etching back said first metal diffusion barrier layer using said third and second insulating layers as a mask;

burying a second metal layer in said trench and via hole, after said first metal diffusion barrier layer is etched back;

diffusing second silicon into said second metal layer from an upper surface thereof so that said second

metal layer is converted into a second silicon-diffused metal layer; and

forming a second metal diffusion barrier layer on said second silicon-diffused metal layer and said third insulating interlayer.

123. The method as set forth in claim 122, wherein said second insulating interlayer comprises at least one of a SiO_2 layer, a SiCN layer, a SiC layer, a SiOC layer and a low-k material layer.

124. The method as set forth in claim 123, wherein said low-k material layer comprises one of a ladder-type hydrogen siloxane layer and a porous ladder-type hydrogen siloxane layer.

125. The method as set forth in claim 124, wherein said ladder-type hydrogen siloxane layer comprises an L-Ox™ layer.

126. The method as set forth in claim 124, wherein said ladder-type hydrogen siloxane layer has a density of about 1.50 g/cm^3 to 1.58 g/cm^3.

127. The method as set forth in claim 124, wherein said ladder-type hydrogen siloxane layer has a refractive index of about 1.38 to 1.40 at a wavelength of about 633 nm.

128. The method as set forth in claim 124, further comprising a step of forming a mask insulating layer made of silicon dioxide on the one of said ladder-type hydrogen siloxane layer and said porous ladder-type hydrogen siloxane layer.

129. The method as set forth in claim 122, wherein said second silicon-diffused metal layer has a larger silicon concentration near an upper side thereof than near a lower side thereof.

130. The method as set forth in claim 122, wherein said second silicon-diffused metal layer comprises a silicon-diffused copper layer.

131. The method as set forth in claim 130, wherein a silicon component of said silicon-diffused copper layer is less than 8 atoms %.

132. The method as set forth in claim 122, wherein said second silicon-diffused metal layer comprises a silicon-diffused copper alloy layer including at least one of Al, Ag, W, Mg, Fe, Ni, Zn, Pd, Cd, Au, Hg, Be, Pt, Zr, Ti and Sn.

133. The method as set forth in claim 122, wherein said second metal diffusion barrier layer comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

134. The method as set forth in claim 122, further comprising a step of forming a second etching stopper between said second and third insulating interlayers, said second etching stopper having a trench opposing said trench.

135. The method as set forth in claim 134, wherein said second etching stopper comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

136. The method as set forth in claim 122, wherein said second silicon diffusing step comprises the steps of:

reducing second oxide on said second metal layer; and

exposing said second metal layer with silicon-including gas so that said second metal layer is converted into said second silicon-diffused metal layer.

137. The method as set forth in claim 122, wherein said second silicon diffusing step comprises the steps of:

coating a second oxidation preventing layer on said second metal layer;

removing said second oxidation preventing layer; and

exposing said second metal layer with

silicon-including gas so that said second metal layer is converted into said second silicon-diffused metal layer after or when said second oxidation preventing layer is removed.

138. The method as set forth in claim 137, wherein said silicon-including gas includes inorganic silane gas.

139. The method as set forth in claim 138, wherein said inorganic silane gas includes at least one of SiH_4 gas, Si_2H_6 gas and SiH_2Cl_2 gas.

140. The method as set forth in claim 137, wherein said second oxidation preventing layer comprises a benzotriazole layer.

141. The method as set forth in claim 137, further comprising a step of reducing second oxide on said second metal layer, before said second oxidation preventing layer is coated.

142. The method as set forth in claim 141, wherein said second oxide reducing step uses oxalic acid.

143. The method as set forth in claim 137, wherein said second oxidation preventing layer removing step, said second silicon-including gas exposing step and said second metal diffusion barrier layer forming step are carried out in the same processing apparatus without exposing said semiconductor device to the air.

144. The method as set forth in claim 140, wherein said second oxidation preventing layer removing step is carried out at a temperature of about 250 to 400℃.

145. The method as set forth in claim 140, wherein said second silicon-including gas exposing step is carried out at a temperature of about 250 to 400℃.

146. The method as set forth in claim 140, wherein said second oxidation preventing layer removing step and said second silicon-including gas exposing step are simultaneously carried out at a temperature of about 250 to 400℃ in the same

processing apparatus using said silicon-including gas.

147. The method as set forth in claim 122, wherein said second silicon-diffused metal layer includes no metal silicide.

148. The method as set forth in claim 122, wherein said second silicon-diffused metal layer includes hydrogen.

149. The method as set forth in claim 122, wherein said second silicon-diffused metal layer includes carbon.

150. The method as set forth in claim 54, further comprising the steps of:

forming a second insulating interlayer on said first metal diffusion barrier layer;

forming an etching stopper on said second insulating interlayer;

forming a via hole in said etching stopper, said via hole opposing said groove of said first insulating interlayer;

forming a third insulating interlayer on said etching stopper, after said via hole is formed;

forming a trench in said third insulating interlayer and a via hole in said second insulating interlayer using said etching stopper as a mask, said trench opposing said via hole;

etching back said first metal diffusion barrier layer using said third and second insulating layers as a mask;

burying a second metal layer in said trench and said via hole, after said first metal diffusion barrier layer is etched back;

diffusing second silicon into said second metal layer from an upper surface thereof so that said second metal is converted into a second silicon-diffused metal layer; and

forming a second metal diffusion barrier layer on said second silicon-diffused metal layer and said third insulating interlayer.

151. The method as set forth in claim 150, wherein said second insulating interlayer comprises at least one of a SiO_2 layer, a SiCN layer, a SiC layer, a SiOC layer and a low-k material layer.

152. The method as set forth in claim 151, wherein said low-k material layer comprises one of a ladder-type hydrogen siloxane layer and a porous ladder-type hydrogen siloxane layer.

153. The method as set forth in claim 152, wherein said ladder-type hydrogen siloxane layer comprises an L-Ox™ layer.

154. The method as set forth in claim 152, wherein said ladder-type hydrogen siloxane layer has a density of about 1.50 g/cm^3 to 1.58 g/cm^3.

155. The method as set forth in claim 152, wherein said ladder-type hydrogen siloxane layer has a refractive index of about 1.38 to 1.40 at a wavelength of about 633 nm.

156. The method as set forth in claim 152, further comprising a step of forming a mask insulating layer made of silicon dioxide on the one of said ladder-type hydrogen siloxane layer and said porous ladder-type hydrogen siloxane layer.

157. The method as set forth in claim 150, wherein said second silicon-diffused metal layer has a larger silicon concentration near an upper side thereof than near a lower side thereof.

158. The method as set forth in claim 150, wherein said second silicon-diffused metal layer comprises a silicon-diffused copper layer.

159. The method as set forth in claim 158, wherein a silicon component of said silicon-diffused copper layer is

less than 8 atoms %.

160. The method as set forth in claim 150, wherein said second silicon-diffused metal layer comprises a silicon-diffused copper alloy layer including at least one of Al, Ag, W, Mg, Fe, Ni, Zn, Pd, Cd, Au, Hg, Be, Pt, Zr, Ti and Sn.

161. The method as set forth in claim 150, wherein said second metal diffusion barrier layer comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

162. The method as set forth in claim 150, wherein said second silicon diffusing step comprises the steps of:

reducing second oxide on said second metal layer; and

exposing said second metal layer with silicon-including gas so that said second metal layer is converted into said second silicon-diffused metal layer.

163. The method as set forth in claim 150, wherein said second silicon diffusing step comprises the steps of:

coating a second oxidation preventing layer on said second metal layer;

removing said second oxidation preventing layer; and

exposing said second metal layer with silicon-including gas so that said second metal layer is converted into said second silicon-diffused metal layer after or when said second oxidation preventing layer is removed.

164. The method as set forth in claim 163, wherein said silicon-including gas includes inorganic silane gas.

165. The method as set forth in claim 164, wherein said inorganic silane gas includes at least one of SiH_4 gas, Si_2H_6 gas and SiH_2Cl_2 gas.

166. The method as set forth in claim 165, wherein said

second oxidation preventing layer comprises a benzotriazole layer.

167. The method as set forth in claim 165, further comprising a step of reducing second oxide on said second metal layer, before said second oxidation preventing layer is coated.

168. The method as set forth in claim 167, wherein said second oxide reducing step uses oxalic acid.

169. The method as set forth in claim 165, wherein said second oxidation preventing layer removing step, said second silicon-including gas exposing step and said second metal diffusion barrier layer forming step are carried out in the same processing apparatus without exposing said semiconductor device to the air.

170. The method as set forth in claim 166, wherein said second oxidation preventing layer removing step is carried out at a temperature of about 250 to 400℃.

171. The method as set forth in claim 166, wherein said second silicon-including gas exposing step is carried out at a temperature of about 250 to 400℃.

172. The method as set forth in claim 166, wherein said second oxidation preventing layer removing step and said second silicon-including gas exposing step are simultaneously carried out at a temperature of about 250 to 400℃ in the same processing apparatus using said silicon-including gas.

173. The method as set forth in claim 150, wherein said second silicon-diffused metal layer includes no metal silicide.

174. The method as set forth in claim 150, wherein said second silicon-diffused metal layer includes hydrogen.

175. The method as set forth in claim 150, wherein said second silicon-diffused metal layer includes carbon.

176. The method as set forth in claim 54, further

comprising the steps of:

forming a second insulating interlayer on said first metal diffusion barrier layer;

forming an etching stopper on said second insulating interlayer;

forming a third insulating interlayer for said etching stopper;

forming a trench in said third insulating interlayer using said etching stopper, said trench opposing said groove of said first insulating interlayer;

etching back said etching stopper, after said trench is perforated;

forming a via hole in said second insulating interlayer using said etching stopper as a mask, said via hole opposing said groove;

etching back said first metal diffusion barrier layer using said third and second insulating layers as a mask;

burying a second metal layer in said trench and said via hole after said first metal diffusion barrier layer is etched back;

diffusing second silicon into said second metal layer from an upper surface thereof so that said second metal layer is converted into a second silicon-diffused metal layer; and

forming a second metal diffusion barrier layer for said second silicon-diffused metal layer and said third insulating interlayer.

177. The method as set forth in claim 176, wherein said second insulating interlayer comprises at least one of a SiO_2 layer, a SiCN layer, a SiC layer, a SiOC and a low-k material layer.

178. The method as set forth in claim 177, wherein said

low-k material layer comprises one of a ladder-type hydrogen siloxane layer and a porous ladder-type hydrogen siloxane layer.

179. The method as set forth in claim 178, wherein said ladder-type hydrogen siloxane layer comprises an L-Ox™ layer.

180. The method as set forth in claim 178, wherein said ladder-type hydrogen siloxane layer has a density of about 1.50 g/cm^3 to 1.58 g/cm^3.

181. The method as set forth in claim 178, wherein said ladder-type hydrogen siloxane layer has a refractive index of about 1.38 to 1.40 at a wavelength of about 633 nm.

182. The method as set forth in claim 178, further comprising a step of forming a mask insulating layer made of silicon dioxide on the one of said ladder-type hydrogen siloxane layer and said porous ladder-type hydrogen siloxane layer.

183. The method as set forth in claim 176, wherein said second silicon-diffused metal layer has a larger silicon concentration near an upper side thereof than near a lower side thereof.

184. The method as set forth in claim 176, wherein said second silicon-diffused metal layer comprises a silicon-diffused copper layer.

185. The method as set forth in claim 184, wherein a silicon component of said silicon-diffused copper layer is less than 8 atoms %.

186. The method as set forth in claim 176, wherein said second silicon-diffused metal layer comprises a silicon-diffused copper alloy layer including at least one of Al, Ag, W, Mg, Fe, Ni, Zn, Pd, Cd, Au, Hg, Be, Pt, Zr, Ti and Sn.

187. The method as set forth in claim 176, wherein said second metal diffusion barrier layer comprises at least one

of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

188. The method as set forth in claim 176, wherein said second silicon diffusing step comprises the steps of:

reducing second oxide on said second metal layer; and

exposing said second metal layer with silicon-including gas so that said second metal layer is converted into said second silicon-diffused metal layer.

189. The method as set forth in claim 176, wherein said second silicon diffusing step comprises the steps of:

coating a second oxidation preventing layer on said second metal layer;

removing said second oxidation preventing layer; and

exposing said second metal layer with silicon-including gas so that said second metal layer is converted into said second silicon-diffused metal layer after or when said second oxidation preventing layer is removed.

190. The method as set forth in claim 189, wherein said silicon-including gas includes inorganic silane gas.

191. The method as set forth in claim 190, wherein said inorganic silane gas includes at least one of SiH_4 gas, Si_2H_6 gas and SiH_2Cl_2 gas.

192. The method as set forth in claim 189, wherein said second oxidation preventing layer comprises a benzotriazole layer.

193. The method as set forth in claim 189, further comprising a step of reducing second oxide on said second metal layer, before said second oxidation preventing layer is coated.

194. The method as set forth in claim 193, wherein said first oxide reducing step uses oxalic acid.

195. The method as set forth in claim 189, wherein said second oxidation preventing layer removing step, said second silicon-including gas exposing step and said second metal diffusion barrier layer forming step are carried out in the same processing apparatus without exposing said semiconductor device to the air.

196. The method as set forth in claim 192, wherein said first oxidation preventing layer removing step is carried out at a temperature of about 250 to 400℃.

197. The method as set forth in claim 192, wherein said first silicon-including gas exposing step is carried out at a temperature of about 250 to 400℃.

198. The method as set forth in claim 192, wherein said first oxidation preventing layer removing step and said first silicon-including gas exposing step are simultaneously carried out at a temperature of about 250 to 400℃ in the same processing apparatus using said silicon-including gas.

199. The method as set forth in claim 176, wherein said second silicon-diffused metal layer includes no metal silicide.

200. The method as set forth in claim 176, wherein said second silicon-diffused metal layer includes hydrogen.

201. The method as set forth in claim 176, wherein said second silicon-diffused metal layer includes carbon.

202. A method for manufacturing a semiconductor device, comprising the steps of:

forming a first groove in a first insulating interlayer;

burying a first metal layer in said groove;

diffusing first silicon into said first metal layer from an upper surface thereof so that said first metal layer is converted into a first silicon-diffused metal layer including no metal silicide;

forming a first metal diffusion barrier layer on said first silicon-diffused metal layer and said first insulating interlayer;

forming a second insulating interlayer on said first metal diffusion barrier layer, said second insulating interlayer and said first metal diffusion barrier layer having a via hole opposing said groove of said first insulating interlayer;

burying a second metal layer in said via hole;

forming a second metal diffusion barrier layer on said metal layer and said second insulating interlayer;

forming a third insulating interlayer on said second metal diffusion barrier layer, said third insulating interlayer and said second metal diffusion barrier layer having a trench opposing said via hole;

burying a third metal layer in said trench;

diffusing second silicon into said third metal layer from an upper surface thereof so that said third metal layer is converted into a second silicon-diffused metal layer including no metal silicide; and

forming a third metal diffusion barrier layer on said second silicon-diffused metal layer and said third insulating interlayer.

203. A method for manufacturing a semiconductor device, comprising the steps of:

forming a groove in an insulating interlayer;

forming a barrier metal layer in said groove;

burying a copper layer in said groove on said barrier metal layer;

reducing oxide on said copper layer;

exposing said copper layer with silicon-including gas so that said copper layer is converted into a silicon-diffused copper layer including no copper

silicide, after said oxide is reduced; and

forming a copper diffusion barrier layer on said silicon-diffused copper layer and said insulating interlayer,

said oxide reducing step, said silicon-including gas exposing step and said copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air.

204. A method for manufacturing a semiconductor device, comprising the steps of:

forming a groove in an insulating interlayer;

forming a barrier metal layer in said groove;

burying a copper layer in said groove on said barrier metal layer;

coating an oxidation preventing layer made of benzotriazole on said copper layer;

exposing said copper layer with silicon-including gas at a temperature of about 250 to 400℃ so that said copper layer is converted into a silicon-diffused copper layer including no copper silicide while said oxidation preventing layer is removed; and

forming a copper diffusion barrier layer on said silicon-diffused copper layer and said insulating interlayer,

said silicon-including gas exposing step and said copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air.

205. A method for manufacturing a semiconductor device, comprising the steps of:

forming a groove in a first insulating interlayer;

forming a first barrier metal layer in said groove;

burying a first copper layer in said groove on said first barrier metal layer;

reducing first oxide on said first copper layer;

exposing said first copper layer with silicon-including gas so that said first copper layer is converted into a first silicon-diffused copper layer including no copper silicide, after said first oxide is reduced;

forming a first copper diffusion barrier layer on said first silicon-diffused copper layer and said first insulating interlayer;

forming a second insulating interlayer on said first copper diffusion barrier layer;

forming a via hole in said second insulating interlayer and said first copper diffusion barrier layer, said via hole opposing said groove;

forming a second barrier metal layer in said via hole;

burying a second copper layer in said via hole on said second barrier metal layer;

reducing second oxide on said second copper layer;

exposing said second copper layer with silicon-including gas so that said second copper layer is converted into a second silicon-diffused copper layer including no copper silicide, after said second oxide is reduced;

forming a second copper diffusion barrier layer on said second silicon-diffused copper layer and said second insulating interlayer;

forming a third insulating interlayer on said second copper diffusion barrier layer;

forming a trench in said third insulating interlayer and said second copper diffusion barrier layer, said trench opposing said via hole;

forming a third barrier metal layer in said trench;

burying a third copper layer in said trench on said third barrier metal layer;

reducing third oxide on said third copper layer;

exposing said third copper layer with silicon-including gas so that said third copper layer is converted into a third silicon-diffused copper layer including no copper silicide, after said third oxide is reduced; and

forming a third copper diffusion barrier layer on said third silicon-diffused copper layer and said third insulating interlayer,

said first oxide reducing step, said first silicon-including gas exposing step and said first copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air,

said second oxide reducing step, said second silicon-including gas exposing step and said second copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air,

said third oxide reducing step, said third silicon-including gas exposing step and said third copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor

device to the air.

206. A method for manufacturing a semiconductor device, comprising the steps of:

forming a groove in a first insulating interlayer;

forming a first barrier metal layer in said groove;

burying a first copper layer in said groove on said first barrier metal layer;

coating a first oxidation preventing layer made of benzotriazole on said first copper layer;

exposing said first copper layer with silicon-including gas at a temperature of about 250 to 400°C so that said first copper layer is converted into a first silicon-diffused copper layer including no copper silicide while said first oxidation preventing layer is removed;

forming a first copper diffusion barrier layer on said first silicon-diffused copper layer and said first insulating interlayer;

forming a second insulating interlayer on said first copper diffusion barrier layer;

forming a via hole in said second insulating interlayer and said first copper diffusion barrier layer, said via hole opposing said groove;

forming a second barrier metal layer in said via hole;

burying a second copper layer in said via hole on said second barrier metal layer;

coating a second oxidation preventing layer made of benzotriazole on said second copper layer;

exposing said first copper layer with silicon-including gas at a temperature of about 250 to 400°C so that said second copper layer is converted into a second

silicon-diffused copper layer including no copper silicide while said second oxidation preventing layer is removed;

forming a second copper diffusion barrier layer on said second silicon-diffused copper layer and said second insulating interlayer;

forming a third insulating interlayer on said second copper diffusion barrier layer;

forming a trench in said third insulating interlayer and said second copper diffusion barrier layer, said trench opposing said via hole;

forming a third barrier metal layer in said trench;

burying a third copper layer in said trench on said third barrier metal layer;

coating a third oxidation preventing layer made of benzotriazole on said third copper layer;

exposing said third copper layer with silicon-including gas at a temperature of about 250 to 400℃ so that said third copper layer is converted into a third silicon-diffused copper layer including no copper silicide while said third oxidation preventing layer is removed; and

forming a third copper diffusion barrier layer on said third silicon-diffused copper layer and said third insulating interlayer,

said first silicon-including gas exposing step and said first copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air,

said second silicon-including gas exposing step and said second copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air,

said third silicon-including gas exposing

step and said third copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air.

207. A method for manufacturing a semiconductor device, comprising the steps of:

forming a groove in a first insulating interlayer;

forming a first barrier metal layer in said groove;

burying a first copper layer in said groove on said first barrier metal layer;

reducing first oxide on said first copper layer;

exposing said first copper layer with silicon-including gas so that said first copper layer is converted into a first silicon-diffused copper layer including no copper silicide, after said first oxide is reduced;

forming a first copper diffusion barrier layer on said first silicon-diffused copper layer and said first insulating interlayer;

forming second and third insulating interlayers on said first copper diffusion barrier layer;

forming a via hole in said third and second insulating interlayers said via hole opposing said groove;

forming a trench in said third insulating interlayer, said trench opposing said via hole;

etching back said first copper diffusion barrier layer after said trench is formed;

forming a second barrier metal layer in said trench and said via hole on said first silicon-diffused copper layer;

burying a second copper layer in said trench

and said via hole on said second barrier metal layer;

reducing second oxide on said second copper layer;

exposing said second copper layer with silicon-including gas so that said second copper layer is converted into a second silicon-diffused copper layer including no copper silicide, after said second oxide is reduced; and

forming a second copper diffusion barrier layer on said second silicon-diffused copper layer and said second insulating interlayer,

said first oxide reducing step, said first silicon-including gas exposing step and said first copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air,

said second oxide reducing step, said second silicon-including gas exposing step and said second copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air.

208. A method for manufacturing a semiconductor device, comprising the steps of:

forming a groove in a first insulating interlayer;

forming a first barrier metal layer in said groove;

burying a first copper layer in said groove on said first barrier metal layer;

coating a first oxidation preventing layer copper layer made of benzotriazole on said first copper layer;

exposing said first copper layer with silicon-including gas at a temperature of about 250 to 400°C

so that said first copper layer is converted into a first silicon-diffused copper layer including no copper silicide while said first oxidation preventing layer is removed;

forming a first copper diffusion barrier layer on said first silicon-diffused copper layer and said first insulating interlayer;

forming second and third insulating interlayers on said first copper diffusion barrier layer;

forming a via hole in said third and second insulating interlayers said via hole opposing said groove;

forming a trench in said third insulating interlayer, said trench opposing said via hole;

etching back said first copper diffusion barrier layer after said trench is formed;

forming a second barrier metal layer in said trench and said via hole on said first silicon-diffused copper layer;

burying a second copper layer in said trench and said via hole on said second barrier metal layer;

coating a second oxidation preventing layer made of benzotriazole on said second copper layer;

exposing said second copper layer with silicon-including gas at a temperature of about 250 to 400℃ so that said second copper layer is converted into a second silicon-diffused copper layer including no copper silicide while said second oxidation preventing layer is removed; and

forming a second copper diffusion barrier layer on said second silicon-diffused copper layer and said second insulating interlayer,

said first silicon-including gas exposing step and said first copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air,

said second silicon-including gas exposing step and said second copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air.

209. A method for manufacturing a semiconductor device, comprising the steps of:

forming a groove in a first insulating interlayer;

forming a first barrier metal layer in said groove;

burying a first copper layer in said groove on said first barrier metal layer;

reducing first oxide on said first copper layer;

exposing said first copper layer with silicon-including gas so that said first copper layer is converted into a first silicon-diffused copper layer including no copper silicide, after said first oxide is reduced;

forming a first copper diffusion barrier layer on said first silicon-diffused copper layer and said first insulating interlayer;

forming a second insulating interlayer and an etching stopper on said first copper diffusion barrier layer;

forming a via hole in said etching stopper, said via hole opposing said groove;

forming a third insulating interlayer on said etching stopper, after said via hole is formed;

forming a trench in said third insulating interlayer and a via hole in said second insulating interlayer using said etching stopper as a mask, said trench opposing said via hole;

etching back said first copper diffusion

barrier layer after said trench is formed;

forming a second barrier metal layer in said trench and said via hole on said first silicon-diffused copper layer;

burying a second copper layer in said trench and said via hole on said second barrier metal layer;

reducing second oxide on said second copper layer;

exposing said second copper layer with silicon-including gas so that said second copper layer is converted into a second silicon-diffused copper layer including no copper silicide, after said second oxide is reduced; and

forming a second copper diffusion barrier layer on said second silicon-diffused copper layer and said second insulating interlayer,

said first oxide reducing step, said first silicon-including gas exposing step and said first copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air,

said second oxide reducing step, said second silicon-including gas exposing step and said second copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air.

210. A method for manufacturing a semiconductor device, comprising the steps of:

forming a groove in a first insulating interlayer;

forming a first barrier metal layer in said groove;

burying a first copper layer in said groove on

said first barrier metal layer;

coating a first oxidation preventing layer made of benzotriazole on said first copper layer;

exposing said first copper layer with silicon-including gas so that said first copper layer is converted into a first silicon-diffused copper layer including no copper silicide while said first oxidation preventing layer is removed;

forming a first copper diffusion barrier layer on said first silicon-diffused copper layer and said first insulating interlayer;

forming a second insulating interlayer and an etching stopper on said first copper diffusion barrier layer;

forming a via hole in said etching stopper, said via hole opposing said groove;

forming a third insulating interlayer on said etching stopper, after said via hole is formed;

forming a trench in said third insulating interlayer and a via hole in said second insulating interlayer using said etching stopper as a mask, said trench opposing said via hole;

etching back said first copper diffusion barrier layer after said trench is formed;

forming a second barrier metal layer in said trench and said via hole on said first silicon-diffused copper layer;

burying a second copper layer in said trench and said via hole on said second barrier metal layer;

coating a second oxidation preventing layer made of benzotriazole on said second copper layer;

exposing said second copper layer with silicon-including gas at a temperature of about 250 to 400℃ so that said second copper layer is converted into a second

silicon-diffused copper layer including no copper silicide while said second oxidation preventing layer is heated; and

forming a second copper diffusion barrier layer on said second silicon-diffused copper layer and said second insulating interlayer,

said first silicon-including gas exposing step and said first copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air,

said second silicon-including gas exposing step and said second copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air.

211. A method for manufacturing a semiconductor device, comprising the steps of:

forming a groove in a first insulating interlayer;

forming a first barrier metal layer in said groove;

burying a first copper layer in said groove on said first barrier metal layer;

reducing first oxide on said first copper layer;

exposing said first copper layer with silicon-including gas so that said first copper layer is converted into a first silicon-diffused copper layer including no copper silicide, after said first oxide is reduced;

forming a first copper diffusion barrier layer on said first silicon-diffused copper layer and said first insulating interlayer;

forming a second insulating interlayer, an etching stopper and a third insulating interlayer on said

first copper diffusion barrier layer;

forming a trench in said third insulating interlayer said trench opposing said groove;

etching back said etching stopper after said trench is formed;

forming a via hole in said second insulating interlayer, said via hole opposing said groove;

etching back said first copper diffusion barrier layer after said via hole is formed;

forming a second barrier metal layer in said trench and said via hole on said first silicon-diffused copper layer;

burying a second copper layer in said trench and said via hole on said second barrier metal layer;

reducing second oxide on said second copper layer;

exposing said second copper layer with silicon-including gas so that said second copper layer is converted into a second silicon-diffused copper layer including no copper silicide, after said second oxide is reduced; and

forming a second copper diffusion barrier layer on said second silicon-diffused copper layer and said second insulating interlayer,

said first oxide reducing step, said first silicon-including gas exposing step and said first copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air,

said second oxide reducing step, said second silicon-including gas exposing step and said second copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor

device to the air.

212. A method for manufacturing a semiconductor device, comprising the steps of:

forming a groove in a first insulating interlayer;

forming a first barrier metal layer in said groove;

burying a first copper layer in said groove on said first barrier metal layer;

coating a first oxidation preventing layer made of benzotriazole on said first copper layer;

exposing said first copper layer with silicon-including gas at a temperature of about 250 to 400°C so that said first copper layer is converted into a first silicon-diffused copper layer including no copper silicide while said first oxidation preventing layer is removed;

forming a first copper diffusion barrier layer on said first silicon-diffused copper layer and said first insulating interlayer;

forming a second insulating interlayer, an etching stopper and a third insulating interlayer on said first copper diffusion barrier layer;

forming a trench in said third insulating interlayer said trench opposing said groove;

etching back said etching stopper after said trench is formed;

forming a via hole in said second insulating interlayer, said via hole opposing said groove;

etching back said first copper diffusion barrier layer after said via hole is formed;

forming a second barrier metal layer in said trench and said via hole on said first silicon-diffused copper layer;

burying a second copper layer in said trench and said via hole on said second barrier metal layer;

coating a second oxidation preventing layer made of benzotriazole on said second copper layer;

exposing said second copper layer with silicon-including gas at a temperature of about 250 to 400°C so that said second copper layer is converted into a second silicon-diffused copper layer including no copper silicide while said second oxidation preventing layer is removed; and

forming a second copper diffusion barrier layer on said second silicon-diffused copper layer and said second insulating interlayer,

said first silicon-including gas exposing step and said first copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air,

said second silicon-including gas exposing step and said second copper diffusion barrier layer forming step being carried out in the same processing apparatus without exposing said semiconductor device to the air.